REMARKS

This Amendment is submitted under 37 C.F.R. § 1.111 in response to the Office Action dated January 9, 2004, wherein pending claims 1 – 3 and 5 – 15 were rejected under 35 U.S.C. § 112 as being indefinite, and claims 1 – 3, 5 – 8 and 15 were rejected as being "obvious" under 35 U.S.C. § 103(a) over various combinations of prior art references. Dependent claims 13 and 14 were said to be allowable over the prior art. Claims 4 and 16 – 18 were withdrawn in accordance with a Restriction Requirement. Claim 4 has now been canceled. In this Amendment applicants have amended independent claims 1 and 5 to overcome the rejections, and have added a new claim 19 to present a generic claim of intermediate scope which is generally similar to claims 5 and 16. Claims 1 – 3, 5 – 15 and 19 are pending, and claims 16 – 18 remain withdrawn. Reexamination and reconsideration of the application are respectfully requested.

Citation of References

The examiner states that he has not considered the U.S. patents listed in the patent application as prior art because they were not submitted in a separate paper. Applicants believe that their listing of patents substantially complies with the requirements of 37 C.F.R. § 1.98, and notes that the USPTO no longer requires the submission of copies of U.S. patents. Applicants' position is that the examiner's reliance on MPEP § 609A(1) is misplaced because the MPEP is an internal guidance manual. As such, the MPEP is binding on patent office employees and officials, but is not binding on members of the public because, unlike the Code of Federal Regulations, the MPEP has not been adopted in accordance with strict federal rule-making requirements. Applicants do not read § 1.98 as *requiring* that the disclosure of information be made in a document which is separate from the patent application. Here, the application includes a list of prior art patents, including the name of the lead inventor and the patent number, as required by § 1.98. Although the issue date of the patents is missing, this omission is harmless.

Applicants further note that they have gone beyond the requirements of § 1.98 insofar as they have voluntarily provided a description of each of the prior art patents. Applicants request confirmation that even if the examiner has not read the patents listed, he has read the applicants' patent application including its discussion of the listed prior art patents.

Nonetheless, without admitting any defect in their prior listing, applicants are submitting a new Information Disclosure Statement herewith.

Section 112

Independent Claims 1 and 5 have been amended to address the examiner's § 112 rejection. Specifically, it is now clarified that the step of "transforming" the metal layer into a bonding layer is accomplished using heat and pressure. The claims have also been amended to clarify that the creation of the bonding layer is what causes bonding between the conductive post and the conductive structure, *i.e.,* that there is no bonding step which is distinct from the step of forming the bonding layer. Applicants wish to thank the examiner for his helpful suggestions.

As to claim 5, the examiner raised concern as to whether the "compressing" and "pressing" steps are the same or different. It is believed that this concern is moot in view of the claim amendment. However, applicants note that those skilled in the art would appreciate that the functionality of causing spreading of the polymer material is different than the functionality of causing bonding of the conductive post to the conductive structure. Therefore, while it may be preferred to apply pressure to accomplish both simultaneously, it is not necessary to do so. Thus, for example, a lower level of pressure may be applied, in the absence of any heat, to first cause spreading of the polymer, and thereafter a higher level of pressure may be used in conjunction with heat, to cause bonding. Accordingly, it submitted that it is not necessary, and would be unnecessarily restrictive, to specify that these two operations are performed as one.

Finally, applicants have changed the references to the "bonding" layer so that it is now called the "intermetallic bonding" layer. This change was made to address the examiner's concern for the use of consistent terminology.

Applicants submit that generic claims 1 and 19 are allowable, and therefore, claims 16 – 18, which were withdrawn as being directed to a non-elected species, will be rejoined. Upon rejoinder of claim 16, applicants intend to amend it in the same manner as claim 5.

Traversal of Obviousness Rejection

Claims 1 – 3, 5 – 12 and 15 were rejected as being obvious in view of various combinations of Tung (U.S. Pat. No. 6,578,754), Gallagher et al. (U.S. Pat. No. 5,948,533), Iino

et al. (U.S. Pat. No. 6,207,259), Murakami (U.S. Pat. No. 6,133,066), Wang (U.S. Pat. No. 6,467,676) and Stephanowski (U.S. Pat. No. 5,334,260).

Each of the rejections is based, in whole or in part, on the examiner's reasoning is that Tung teaches the use of solder at the ends of pillars or posts for flip chip bonding, and Gallagher et al. and Iino et al. each teach the use of pastes containing powdered solder and powdered metal which react when heated to form intermetallic compounds in a matrix. However, the examiner has failed to show why the teachings of Gallagher et al. and Iino et al. would be combined with Tung. In other words, the examiner has failed to explain why one would use the pastes of secondary references with the structure shown in the primary reference. There is nothing in any of the references suggesting any benefit to this combination. Nor is there anything in any of the references which suggests a benefit to forming an intermetallic bonding layer in the Tung structure.

In order to support an obviousness rejection, it is the examiner's burden to do more than to show that the various elements of the claims exist in the prior art. The examiner is obliged to show there is some suggestion or other motivation for combining the teachings of the prior art in the way which is claimed. The examiner has failed to meet this required burden. Applicants submit there is no reason someone of ordinary skill in the art would have combined the teachings to get the presently claimed invention.

The examiner states that an intermetallic bonding layer is inherently formed when solder is melted in contact with copper. Applicants submit that in a typical soldering operation the amount of intermetallic material produced is so negligible as to be essentially zero, and that this imperceptible intermetallic layer is unimportant in causing bonding. However, applicant has voluntarily amended each of the independent claims so that they all now require that "substantially the entire" thin metal layer is transformed into an intermetallic bonding layer. Support for this amendment is found, for example, in the original application at page 50, lines 6 – 7. ("Due to phase transition, the thin layer 3 is *consumed and transformed* into a high melting point phase or layer 3a" – emphasis added.) Thus, even if a microscopically thin intermetallic layer is inherently formed during the soldering process of Tung, there is no teaching or suggestion that substantially the entire layer be transformed into an intermetallic layer.

The examiner argues that motivation exists to transform the solder layer of Tung into a higher melting point intermetallic layer "in order to provide greater stability for the bond in

subsequent processing as suggested by Gallagher." Applicants submit that to the extent this motivation exists, it is limited to use in structures which undergo *sequential* high temperature processing and, therefore, this motivation would not apply in the context of Tung. Indeed, the examiner's statement highlights important differences between Tung and the secondary references.

Tung is directed to a structure and process for mounting a pre-fabricated *semiconductor chip* on a substrate. The goal of the invention is to ensure that the semiconductor chip is positioned a sufficient distance away from any lead-containing solder so as to avoid bombardment of active electronic devices on the chip by alpha radiation emitted from naturally-occurring lead isotopes in the solder. Accordingly, each of the claims of Tung recite the presence of a semiconductor chip. There is no suggestion that Tung's chips undergo any further high temperature processing after they have been soldered to the chip-carrying substrate. Moreover, it is a well known goal when working with semiconductor chips that it is desirable to have the ability to "rework" the connection in case of a problem. This ability would be essentially eliminated if the solder layer were substantially transformed into a high melting point intermetallic layer.

In contrast, Gallagher et al. and Iino et al. do not involve semiconductor chips. Instead, both patents are directed to techniques for manufacturing printed wiring board assemblies having multiple layers. In each of these patents, conductive pastes are used to form vias that are internal to the wiring board. In one embodiment described in Gallagher et al., the layers of the multilayer substrate are formed sequentially. It is in this sequential processing context, Gallagher et al. discusses the fact that forming a via comprising intermetallic material in a first layer prevents the metal from reflowing during formation of the next layer. Thus, Gallagher et al.'s teaching is expressly limited to the context of "multiple sequentially processed *layers*" (emphasis added), *i.e.,* the only advantage described in Gallagher et al. is in the context of forming a multilayer substrate where the layers are sequentially formed. This teaching has no application to the primary reference, Tung.

Both Gallagher et al. and Iino et al. disclose that very long processing times for forming the intermetallic vias of their respective inventions. (See, for example, Iino et al.'s Table 1, showing heat treatment times ranging between 1 – 5 hours.) In view of the critical importance of manufacturing throughput, anyone adopting Tung's chip mounting technique would want to

minimize the processing time, rather than extend it. Forming a solder joint taking only seconds. Substantially transforming an entire solder layer into a intermetallic layer takes considerably more time and, as noted above, is essentially irreversible.

Independent claims 1 and 5, as amended, further require that heat *and* pressure be used to form the intermetallic bonding layer. There is no suggestion or motivation shown for applying pressure during the soldering step of Tung. Tung's copper posts are very narrow in diameter – the patent suggests that the pitch, *i.e.,* the center-to-center spacing between adjacent pillars is preferably in the range of 80 – 100 microns, meaning that the diameters of the pillars are significantly narrower than this amount. Since 100 microns is a tenth of a millimeter, it is clear that Tung's pillars are very narrow. Application of pressure to pillars of copper that are less than a tenth of a millimeter in diameter would almost certainly cause bending or warpage of the pillars. Thus, it is submitted it that the use of pressure in Tung's process would be studiously avoided.

In the Office Action, the examiner states that Tung teaches that "the flip chip is bonded to a substrate under heat and pressure ..." (Office Action, paragraph 7). Applicants could find no mention in Tung concerning the application of pressure during the soldering process. Tung's soldering process is described at column 5, lines 25 – 31, which reads: "To connect the pillars to the substrate, portions **16***b'* are *placed in contact* with the copper contacts **22** on the substrate **14** as shown in FIG. 2F. The portions **16***b'* containing solder are then heated in a manner known to those skilled in the art to reflow the solder **16***b'* to form solder portions **16***b* and pillars **16** as shown in FIGS. 1B and 2G. An underfill material ..." (Emphasis added.) Likewise, Tung's "Summary of the Invention" states: "After the pillars have been formed, the pillars may be connected to the substrate by *placing the pillars in contact* with the substrate and heating the solder until the solder reflows." (Column 3, lines 31 – 34; emphasis added.) There is no indication that pressure is *applied* during the soldering process. The word "pressure" does not appear anywhere in the patent. As noted above, there is very good reason why pressure would *not* be used in the Tung soldering process.

Similarly, in paragraph 8, page 8, the examiner refers to Tung's "lamination step". Applicants point out that the words "laminate" or "lamination" do not appear anywhere in the Tung patent. If the examiner is suggesting that "lamination" implies the application of pressure, there is no basis in the Tung patent for saying that it teaches a "lamination step".

As to claim 5, combining the teachings of four different references the examiner states that it would have been obvious to modify Tung's underfill process to instead place a liquid polymer on the substrate prior to placing the semiconductor chip on the substrate. Moreover, the examiner asserts that it would have been obvious to place the liquid polymer away from the edges of the substrate and cause it to spread outwardly. Applicants respectfully disagree, and submit that the examiner has not shown any motivation for making this change. As discussed above, Tung teaches making contact between his pillars and his pads by "placing" the chip on the substrate, and it would be disadvantageous to apply pressure because of the risk of bending the very narrow diameter pillars. If the liquid polymer were deposited on the substrate prior to the soldering step, it would be necessary to apply pressure to ensure that the pillars penetrated through the viscous liquid polymer to make good electrical contact with the pads. In addition, the claim requirement that the polymer be spread towards the edges would be potentially problematic for Tung, insofar as the outward spreading would result in a lateral force being applied to the pillars which might cause bending. Thus, when using the Tung process, one would have avoided application of a liquid polymer until after the soldering process was completed. This is all that is taught in Tung, and there is no reason shown to modify Tung.

It is further noted that in the Office Action the examiner takes the position that it does not matter whether the solder layer is placed on the post or on the conductive structure. This position is directly contrary to the examiner's unequivocal assertion, in the Restriction Requirement, that claim 5 is patentably distinct from claim 16. The examiner cannot have it both ways: in one Office Action (the Restriction) saying that the placement of the solder layer (which is the only essential difference between original claims 5 and 16) is patentably distinct, yet in the subsequent Office Action asserting that the difference is obvious and, *at the same time,* finalizing the restriction.

New Claim 19

New claim 19 has been added to provide a generic claim of intermediate scope. Claim 19 is similar to claim 5, but specifies that the thin metal layer can be formed *either* on the conductive post *or* on the conductive structure. Likewise, claim 19 specifies that the liquid polymeric material is placed on one or the other of the two substrates before they are placed in

contact with one another. It is a matter of design choice as to which of the substrates receives the polymer before being joined.

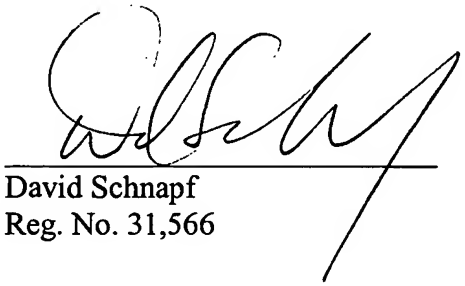
Conclusion

In view of the foregoing amendments and remarks, Applicants submit that the application is now in condition for allowance and such action is earnestly solicited. The examiner is invited to telephone the undersigned at the below-listed number if doing so would advance the prosecution of the application

April 8, 2004

Sheppard Mullin Richter & Hampton LLP
4 Embarcadero Center
17th Floor
San Francisco, CA 94111-4106
Tel: (415) 434-9100
Fax: (415) 434-3947

Respectfully submitted,



David Schnapf
Reg. No. 31,566